REMARKS

In response to the final Office Action dated November 6, 2002, Applicants have submitted concurrently herewith a Request for Continued Examination along with the instant Amendment. In regard to the first point raised in the Office Action, the Examiner has asserted that the Applicant received an action on the merits for the originally presented invention drawn to a process and that the invention has been constructively elected by the original presentation for prosecution on the merits.

However, Applicant notes that preamble of claims 1-7 clearly state that the claimed subject matter in those claims was a multi-layer semiconductor device assembly jig and that remaining claims 8-10 are directed to corresponding method claims. Applicant submits that by receiving the original Office Action and responding on the initial claims there was no constructive election as asserted by the Examiner. Furthermore, Applicants note that where search and examination of the entire application may be made without undue burden to the Examiner, it is appropriate to examine all claims in a single application. Here, in the present circumstance, a search and examination of the method claims would necessarily entail corresponding search of any art relevant to the apparatus claims. In light of the foregoing, Applicants respectfully request the Examiner reconsider the assertion of construction election. Accordingly, Applicants have submitted modified claims 1-7 as well as 8-10 for reconsideration by the Examiner.

Applicants respectfully request reconsideration of the prior art rejection set forth by the Examiner under 35 U.S.C. §§102 and 103. Applicant respectfully submits that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's presently claimed invention. Applicant's claimed invention is directed to new and improved structures and method of manufacturing semiconductor devices wherein semiconductor chips are secured through printed wiring board members and thereafter a stack of the printer wiring board members are further processed in an assembly jig which ensures that the resultant stacked chip module has improved characteristics including better connections between individual members within the module and a corresponding improvement in reliability.

Applicants submit that the art of record is much different than that which is disclosed and claimed by Applicants in the present application. For example, the Levy reference, United States Patent No. 5,869,353 is merely directed to a modular panel stacking process

wherein chips are initially encapsulated in a plastic housing and leads arranged around the periphery of the chips are secured through frame members and the frame members are stacked. Thereafter, the frames are cut to provide stacked chip modules. At the very least, this reference is different from Applicants in that there is no teaching or suggestion whatsoever regarding the use of printed wiring board members in such a stack.

One particular advantage of Applicant's disclosed use of the printed wiring board members is the fact that interconnections between the printed wiring board members can be achieved without the use of a contact from one of the chip members. This may be particularly advantageous where electrical communication between non-adjacent chips in a stack module is desired. In the Levy reference, the only way in which this could be achieved would be if a dummy lead were utilized by one of the chip members but this is obviously less desirable than being able to make such a connection through contacts on the printed wiring board members themselves without the need for utilizing a dummy lead from an actual chip.

One particular advantage is the obvious design flexibility that is provided through Applicant's disclosed invention. Applicant submits that the remaining references of record similarly fail to provide any teaching or suggestion whatsoever regarding the advantageous use of printer wiring board members as disclosed and claimed now in the instant application. Accordingly, in light of the foregoing, Applicant respectfully requests reconsideration of the claims in light of the foregoing amendments.

Respectfully submitted,

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1. A multilayer semiconductor device assembly jig, comprising:

a lateral position restriction mechanism for positioning a plurality of stacked semiconductor modules on a base member with their respective lateral positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member; and

an alignment mechanism for providing alignment with reference to a mother substrate and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by holder connections between top and bottom surfaces thereof.

2. The multilayer semiconductor device assembly jig according to claim 1 comprising a box-shaped member which is positioned on said base member and having a storage space for storing said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said lateral position restriction mechanism.

3. The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said box-shaped member and said mother substrate.

4. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules.

5. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins also pierce through a positioning hole formed on said mother substrate.

7. The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism further comprises:

a cover member secured over said semiconductor modules.

8. A multilayer semiconductor device manufacturing method using an assembly jig for mutually restricting positions of a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board comprising the steps of:

serially layering the semiconductor modules on a base member with respective lateral positions restricted by a lateral position restriction mechanism and placing said assembly jig with an entire height of said layered modules restricted by said height restriction mechanism,

supplying said assembly jig into a reflow furnace, applying reflow heating to melt solder bumps and for thereby forming interlayer connection among said semiconductor modules, and thus forming a layered semiconductor module unit; and

mounting said layered semiconductor module unit on a mother substrate by using a top-layer semiconductor module as a junction module and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by holder connections between top and bottom surfaces thereof..

9. The multilayer semiconductor device manufacturing method according to claim 8, further comprising a step of providing said assembly jig with an alignment mechanism for aligning said layered semiconductor module unit against said mother substrate.

10. The multilayer semiconductor device manufacturing method according to claim 8 further comprising the step of:

forming a bump on each of connection lands and dummy lands of printed wiring board for each semiconductor module.